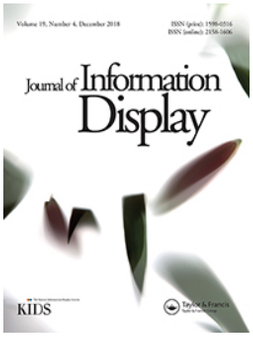

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Low-temperature poly Si TFTs via BLDA for a Ne-sputtered Si film using sputtered gate SiO_2

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ABSTRACT

Amorphous SiO_2 and amorphous Si films were deposited on glass using radio frequency (RF) sputtering, and were subsequently poly-crystallized using blue-laser diode annealing (BLDA) scanned by a CW beam. Ne, which has a smaller atomic radius than Ar, was used for the sputtering of the Si film. For the gate insulator, a small amount of O_2 gas diluted with Ar was flown during the sputtering to optimize the SiO_2 film with a low leakage current. A simple TFT structure with a metal source and drain (S/D) was adopted to realize a low-temperature process with a low fabrication cost. Furthermore, to confirm the effectiveness of the sputtered gate oxide, a poly-Si TFT adopting a Si film deposited using plasma-enhanced chemical vapor deposition (PE CVD) for the channel was fabricated and was compared with the TFT with a sputtered Si film for the channel. Reasonable V_g-I_d characteristics were obtained for both poly-Si TFTs. The TFT structure with a metal S/D formed through a low-temperature sputtering-based process is expected to be applied to Si TFTs on an arbitrary flexible panel.

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TFT; poly Si; sputtering; gate oxide

1. Introduction

Low-temperature poly-Si (LTPS) thin-film transistors (TFTs) [1–3] have been extensively studied for application in the active-matrix liquid crystal display (AM LCD) and the active-matrix organic light-emitting diode (AM OLED) display on glass even on flexible panels [4, 5]. The LTPS TFT fabrication process makes it possible to integrate peripheral driving circuits on an identical panel. Flexible or bendable use is currently desired for the next-generation smart display panel, which mounts high-performance TFTs on polymer plastic sheets. For the fabrication of poly-Si TFTs on plastic, a fairly low-temperature (below 500°C) fabrication process is required. Although a transfer process onto a polymer plastic sheet after the fabrication of TFTs on a glass substrate has been proposed and developed, the fabrication cost for the technique of removing the TFT layer from glass substrate by laser exposure is an issue for practical production [6]. For the low-temperature fabrication of the poly-Si TFT system on plastic, the de-hydrogenation annealing step before excimer laser annealing (ELA) for the Si film deposited using plasma-enhanced chemical vapor deposition (PE CVD) limits the maximum process temperature of the TFT. For sputtered Si deposition, although there are no hydrogen atoms in the film, Ar and O atoms are incorporated into the Si film as impurity contaminants, which restricts the crystal grain growth through laser annealing [7]. Promising poly-crystallization results for a direct current (DC)-sputtered Si film have been reported [8, 9], and the radio frequency (RF)-sputtered technique should be more favorable, including the deposition of a gate insulator film as an LTPS TFT fabrication process.

The authors have reported blue-laser diode annealing (BLDA) as a new LTPS TFT fabrication process [10, 11]. A Si film consisting of uniform micrograins with improved electrical properties can be formed reproducibly, and the surface can be kept smooth by adopting scanned BLDA for amorphous Si films [11–13], which can hardly be formed by the conventional pulsed ELA. For high-quality CVD Si films, anisotropic long grains along the scanning direction of the laser beam can be obtained [11, 14]. Furthermore, for the PE CVD amorphous Si films, smooth poly-Si films have been obtained via BLDA even without performing the de-hydrogenation annealing, which reduces the maximum process temperature of the TFT [15]. To realize the poly-Si TFT system on a polymer sheet using laser crystallization, an interlayer structure between an amorphous Si film and under plastic sheet should be designed to

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avoid thermal damage. Thus, as the crystallization of a Si film on a flexible plastic via BLDA as well as via ELA has been realized [16, 17], a low-temperature process for TFT fabrication is expected and should be optimized.

2. Experiment

50-nm-thickness amorphous Si films were deposited on glass via RF sputtering. To study the effect of the impurity species incorporated into a Si film on the crystallization behavior using BLDA, a heavily phosphorus-doped Si film was deposited via RF sputtering using Ne or Ar as the sputtered gas against a single-crystalline Si target with low resistivity (0.0013–0.0016 Ωcm, $\sim 6 \times 10^{19}$ cm^{-3}). As a result [18], the sheet resistance of the Si films irradiated above the 4 W condition was drastically decreased for both the cases of Ne and Ar sputtered deposition, and the obtained values are lower for the Ne case than for the Ar case, as shown in Figure 1. By adopting Ne as the sputtering gas, the maximum endured laser power for the Si film was extended towards a much higher power. Thus, not only small grains but also larger grains with slightly anisotropic long grains, as shown in the CVD Si film [10, 14], can be stably obtained even for the sputtered Si film.

Top-gate-structured poly-Si TFTs with a metal source and drain (S/D) poly-crystallized using BLDA were fabricated based on a low-temperature process on glass [19]. For the TFT fabrication, a 50-nm-thick Si film was deposited via RF sputtering. Subsequently, a 2.4×600 μm 445 nm laser beam was scanned at 500 mm/s. After patterning the channel, Ti was evaporated in vacuum. In addition, a 50-nm-thick gate SiO_2 was deposited via RF sputtering. Finally, Al electrodes for the gate and S/D were formed through the contact hole connecting to the Ti surface. The whole process was limited to below 400°C for the sintering using forming gas (H_2/N_2) after Al electrode formation.

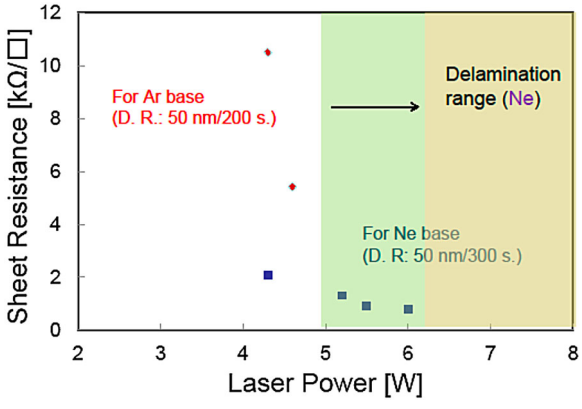

Figure 1. Sheet resistance after BLDA for the sputtered doped Si films using Ar or Ne gas [18].

For the channel Si, intrinsic n^- single-crystal Si was used as the target, and Ne gas was used during the RF sputtering under a deposition condition similar to that for the heavily doped film described above. The Ne atoms in the Si film are expected to effuse out much easier during heating through BLDA as the atomic radius of Ne is smaller than that of Ar. After BLDA at 5 W for a sputtered Si film, a Si film with comparatively smaller poly-Si grains compared to a CVD film is formed.

Additionally, a poly-Si TFT using a CVD Si film for the channel was fabricated for comparison with the device performance formed using an RF-sputtered Si film for the channel. In these two TFTs, a gate SiO_2 was formed via RF sputtering using SiO_2 as the target [19]. As an a-Si film deposited by a PE CVD film at below 300°C has a high hydrogen atom content, the Si film was subjected to de-hydrogenated annealing at 500°C for 1 h in N_2 ambient before BLDA to obtain a high-crystal structure for the Si film. Except for the hydrogenation annealing, the TFT process temperature was kept at below 400°C, the same as for the TFT with a sputtered Si channel. After the deposition of Si films on glass, the size of the 445 nm blue-laser beam was kept at 600×2.4 μm^2, and the Si films were crystallized by keeping the output power at 5 W. The crystallinity of the Si film was analyzed through spectroscopic ellipsometry (SE).

After patterning the channel Si layer, Ti was deposited using vacuum evaporation for an S/D similar to the TFT with a sputtered Si channel described above. By using a metal with a low work function, a quasi-ohmic contact barrier for electrons is realized. The work function of Ti is known as 4.33 eV, and the electron affinity of single-crystalline Si is 4.05 eV; thus, the resultant barrier for electrons is lowered even for Ti/poly-Si contact if the states' density on the poly-Si surface relating to grain boundaries, etc. is considerably reduced by terminating with hydrogen atoms. The device structure with a metal S/D is shown in Figure 2 [19].

For the gate insulator, about 100-nm-thick SiO_2 film was deposited at room temperature via RF sputtering

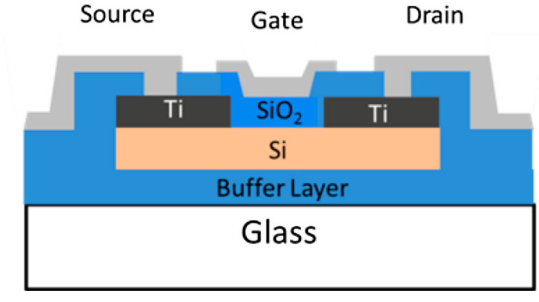

Figure 2. Cross-section of the fabricated TFT [15, 19, 24].

using O_2 gas flow mixed with Ar (Ar: 10 sccm; O_2: 3 sccm) [20–22]. After patterning the SiO_2 for contact holes, Al electrodes were evaporated in vacuum.

To evaluate the fundamental electrical performance of the SiO_2 film, such as the leakage current and the capacitance-voltage (C-V) characteristic, in addition to TFT, a capacitor diode with an Al/SiO_2/single-crystal Si structure was formed. A 0.5-mm φ ($\sim 2 \times 10^{-3}$ cm^2) Al electrode was evaporated on the SiO_2/Si wafer, and the C-V characteristic was evaluated.

TFT fabrication for the RF-sputtered Si film was conducted through a low-temperature (below 400°C) process, using a sputtered SiO_2 gate [23, 24]. For the TFT using a PE CVD Si film with a metal S/D, the process temperature was also limited to below 400°C, except for the de-hydrogenation annealing at 500°C [24]. After the completion of the TFT fabrication, the transfer curves were measured before and after hydrogen annealing in H_2/N_2 (4%) ambient at 400°C.

3. Results and discussion

Figure 3 shows the extinction coefficient (k) deduced from the SE analysis for the sputtered Si films before and after BLDA at 5 W. As is shown for the extinction coefficient spectrum after BLDA, a peak appeared at around 280 nm, and a fine shoulder was observed at around 360 nm. Once grain growth occurs, an energy band is formed. As a result, the band-to-band absorption probability increased. In the crystalline or crystallized Si, the probability increases drastically at 3.6 and 4.4 eV. Based on the result, the Si film obtained after BLDA had apparently been crystallized. Figure 4 shows the transmission electron microscopy (TEM) image of the poly-Si films sputtered via BLDA at 5 W [19]. The grain size is less than 300 nm, and the film has slightly small defects. In terms of the crystallinity of the Si film, the BLDA for the CVD film was higher than that for the sputtered film. The obtained grain size for the sputtered Si film after annealing is smaller than that for the CVD film. As impurities such as oxygen and sputtered gas (Ne or Ar) are incorporated into the film during the deposition, the grain growth is disturbed even from the melting phase, and the resultant grains contain fine defects. These impurities or fine defects as well as the limited size of the grains may disturb the electrical transport in the film. Sputtering, however, has an advantage for the lower- temperature TFT process.

The crystallinity of the sputtered poly-Si film is inferior to that of the CVD poly-Si film as the obtained grain size of the sputtered Si film was limited after laser annealing [24].

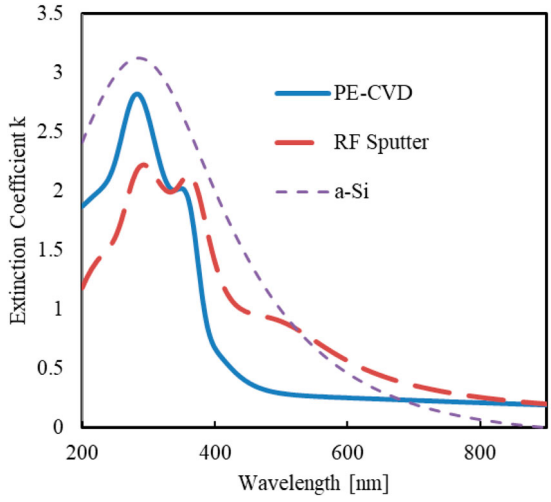

Figure 3. Extinction coefficient spectra of the Si films before and after BLDA [19].

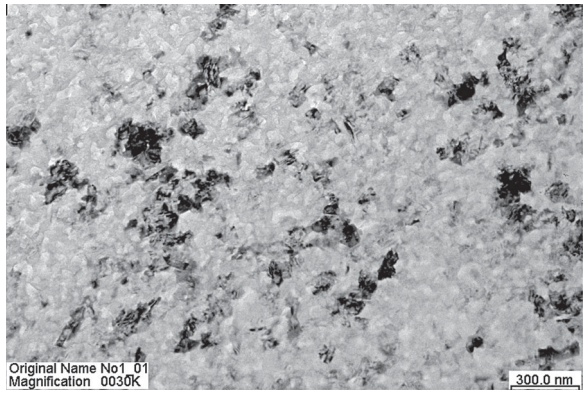

Figure 4. TEM image of the sputtered Si film crystallized via BLDA at 5 W [19].

For the capacitor sample of the gate insulator formed by incorporating O_2 into the Ar flow during the RF-sputtered deposition, SiO_x ($x < 2$) changed to SiO_2 ($x \sim 2$). As a result, the breakdown voltage increased to higher than 7 MV/cm, and the leakage decreased [20, 21]. Figure 5 shows the high-frequency C-V curve of the sputtered SiO_2 sample measured under 100 kHz. After 4% hydrogen annealing at 200°C for 30 min, the hysteresis width (ΔV_{hys}) was reduced from 0.18 to 0.07 V. This result indicates that the defects in the SiO_2 and/or at the SiO_2/Si interface were reduced by hydrogen annealing at 200°C. The defect density can be roughly estimated from the hysteresis width by ($\Delta Q/q = C_{ox} \times \Delta V_{hys}/q$), and the defect density was reduced from 8.0×10^{10} to 3.4×10^{10} cm^{-2}. Correspondingly, the flatband voltage was also improved from −5.2 to −2.5 V; thus, the fixed charge density could be reduced. Here, the ideal value of the flatband voltage using Al and p-type Si wafer of ~ 10Ωcm is around −0.9 V; thus, the shift

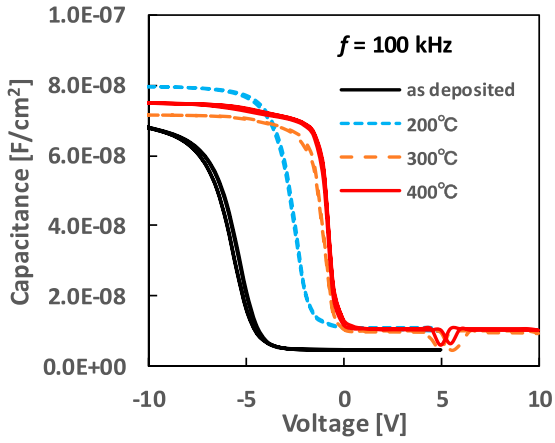

Figure 5. C-V characteristics after hydrogen annealing following the formation of Al electrodes (at 100 kHz for a 2×10^{-3} cm^2 capacitor area) [22].

of the flatband voltage (ΔV_{fb}) was reduced from −4.3 to −1.6 V, and the fixed charge densities in the film ($Q_{defect}/(q \times \text{thickness}) = C_{ox} \times \Delta V_{fb}/(q \times \text{thickness})$) were estimated to be 2.7×10^{24} and 1.0×10^{24} cm^{-3}, respectively. By increasing the temperature to 300°C, a 1.1×10^{10} cm^{-2} defect density and a 4.2×10^{17} cm^{-3} fixed charge density could be obtained, and these values should be further reduced by optimizing the annealing condition.

For the TFT, before the hydrogen annealing at 400°C, the typical TFT characteristic was not obtained both for the sputtering Si film and for the CVD Si film. After the sintered hydrogen annealing, the drain current increased remarkably, the typical TFT characteristics were successfully obtained, and the improvement of the drain current was confirmed. The crystal defects, including the grain boundaries in the Si films and at the Si/SiO_2 interface, are speculated to have been compensated for by the hydrogen atoms. Additionally, hydrogenation is considered to have also affected the gate SiO_2 film itself, as shown in the C-V curve for the metal oxide semiconductor (MOS) capacitor (Figure 5). From the TFT transfer curve, the deduced value of the effective electron mobility after the hydrogen annealing was as high as 50 $cm^2/(Vs)$, the threshold voltage was 1.8 V, and the S factor was 1.3 V/dec at the 0.1 V drain voltage. Figure 6(a) shows the V_g-I_d characteristic of the TFT (L/W = 20 µm/ 5 µm) after hydrogen annealing for 90 min at 400°C.

Additionally, the transfer curve was measured for the TFT fabricated using a PE CVD Si film. A higher drain current was obtained with the TFT using the Si film deposited via PE CVD than that obtained with the TFT using the Si film deposited via sputtering (Figure 6(a), (b)). From the transfer curve, the deduced carrier mobility after the hydrogen annealing was 165 $cm^2/(Vs)$, the threshold voltage was 1.8 V, and the S factor (i.e. gate voltage swing) was 0.5 V/dec at the 0.1 V drain voltage. As the exposed laser power was as low as 5 W, the grain size in the films after BLDA is not large [10, 11], and the crystallinity, which affects the device performance, is lower for the sputtered Si film than for the CVD Si film.

In the case of the RF-sputtered Si film, Ne sputtering is expected to be superior to the Ar sputtering for the poly-Si properties after BLDA, as described above, in the Introduction section. In general, for the sputtering technique, although a much higher amount of an inactive gas with a lighter mass is incorporated into the thin film [25], the gas atom is effused out more efficiently after thermal annealing [7, 26]. To develop a higher-performance TFT system on a flexible polymer sheet, the deposition condition for the sputtering, such as a desirable impurity content and its amorphous phase state for the Si network, should be taken into account to realize an effective crystallization close to the CVD Si film [18, 27]. For the PE

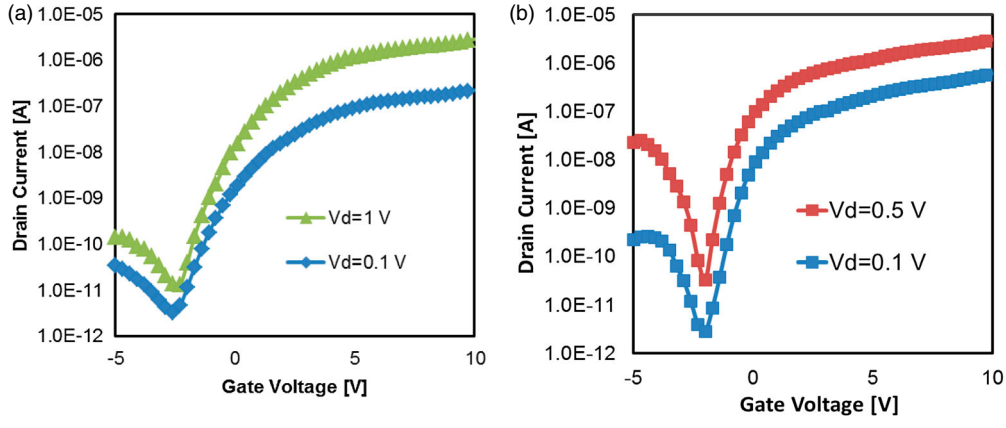

Figure 6. Dependence of the V_g-log I_d characteristic, L/W = 5 µm/10 µm). (a) For the RF-sputtered Si film [19, 24] (b) For the PE CVD Si film [23, 24].

CVD Si film, the p-channel TFT performance was also observed by adopting the high-work-function Au for the metal S/D structure, although the effective hole mobility has a low value (14 cm^2/Vs) [28]. Through the optimization of the deposition through the TFT process, a much higher device performance with a metal S/D structure is expected not only for the CVD Si film but also for the sputtered Si film.

4. Summary

Poly-Si thin-film transistors (TFTs) formed using blue-laser diode annealing (BLDA) at a low temperature with a low-cost process was discussed, based on the sputtered process. For the source and drain, quasi-ohmic contact was formed using Ti, a low-work-function metal, without adopting impurity doping. For the gate insulator, a high-quality sputtered gate SiO_2 film was obtained by optimizing the radio frequency (RF) sputtering. After hydrogen annealing at 400°C, an improved poly-Si TFT characteristic was successfully obtained, and the drain current increased remarkably not only for the sputtered Si film but also for the Si film deposited via chemical vapor deposition (CVD). After adopting the sputtered gate SiO_2, the deduced effective carrier mobility became 50 cm^2/Vs, and the threshold voltage became 2.5 V at the 0.1 V drain voltage, while a 165 cm^2/Vs effective field effect mobility was deduced for the poly-Si TFT using plasma-enhanced (PE) CVD.

The advanced low-temperature poly-Si (LTPS) TFT process is expected to be applied to arbitral panel applications.

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Disclosure statement

No potential conflict of interest was reported by the authors.

Notes on contributors

Takashi Noguchi received his M.S. degree in 1979, and his Ph.D. degree in 1992, from Doshisha University. In 1979, he joined Sony Corp. and contributed to its R&D on Si MOS LSIs and Si TFTs (LTPS). In 1994, he worked as a visiting scientist at MIT. In 1998, he managed a research work on novel Si devices at Sony Research Center. In 2001, he moved to France to work as a research scientist at CNRS in Universite Paris-Sud. In 2002, he moved to South Korea and managed two research projects as an executive member of SAIT, and also contributed to SungKyunKwan University. Since after 2006, he has been a professor of University of the Ryukyus in Japan.

Tatsuya Okada received his Ph.D. degree from Hiroshima University in 2009. He is currently an assistant professor at the Faculty of Engineering, University of the Ryukyus in Japan, and his area of concentration is blue-laser diode annealing for innovative applications. Dr. Okada is a member of the Japan Society of Applied Physics and of the Institute of Electronics, Information, and Communication Engineers.

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